UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,677	03/20/2000	Hiroshi Baba	000348	6236

23850 7590 05/02/2003

ARMSTRONG,WESTERMAN & HATTORI, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER
WILLIAMS, LAWRENCE B

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/531,677	BABA, HIROSHI
	Examiner	Art Unit
	Lawrence B Williams	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art.

(1) With regard to claim 1, Applicant's Admitted Prior Art discloses in Fig. 2, a method of controlling a power saving operation for a phase comparator unit, comprising the steps of: dividing a frequency of a reference signal to generate a reference frequency divided signal; dividing a frequency of an input signal to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; comparing the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; generating a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal; generating a first initializing signal for initializing the output of the step of dividing the frequency of the reference signal in accordance with the power saving state canceling signal; and generating a second initializing signal for initializing the output of the step of dividing the frequency of the input signal in accordance with the power saving state canceling signal (pg. 2, lines 9-37; pg. 3, lines 1-17).

(2) With regard to claim 3, claim 3 inherits all limitations of claim 1.

(3) With regard to claim 5, Applicant's Admitted Prior Art also discloses in Fig. 1, a PLL frequency synthesizer comprising; a phase comparator unit; a loop filter which receives an output of the phase comparator unit; and a voltage control oscillator which receives an output of the loop filter, the phase comparator unit comprising: a reference signal frequency dividing unit 20 which divides a frequency of a reference signal to generate a reference frequency divided signal; a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; a phase comparator

which compares the phases of the reference frequency divided signal and 30 the comparison frequency divided signal so as to output a comparison result; a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal; a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal (pg.1, lines 14-36; pg. 3, lines 9-17).

(4) With regard to claim 7, claim 7 inherits all limitations of claim 5.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 4, 6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art as applied to claims 1, 3, 5, and 7 above, and further in view of Yoshinaka (US Patent 5, 877,657).

(1) With regard to claim 2, as noted above, Applicant's Admitted Prior Art discloses all

limitations of claims 1, 3, 5, and 7. Applicant's Admitted Prior Art does not however, disclose wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other.

However, Yoshinaka teaches a PLL clock generator wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other (col. 5, lines 34-55).

One skilled in the art would have clearly recognized that a PLL clock generator wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Yoshinaka to the invention as described in Applicant's Admitted Prior Art to provide a low cost clock generator, eliminate extra terminals and allow frequency dividing ratios to be freely performed (col. 2, lines 34-40).

(2) With regard to claim 4, claim 4 inherits all limitations of claims 2 and 3.

(3) With regard to claim 6, claim 6 inherits all limitations of claims 2 and 5.

(4) With regard to claim 8, claim 8 inherits all limitations of claims 2 and 7.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Jokura (US Patent 5,541,929).

Applicant's Admitted Prior Art discloses in Fig. 1, a PLL frequency synthesizer comprising: a phase comparator unit; a loop filter which receives an output of the phase comparator unit; and a voltage control oscillator which receives an output of the loop filter, the phase comparator unit comprising: a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal; a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; a phase comparator which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal; a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal (pg.1, lines 14-36; pg. 3, lines 9-17).

However, Applicant's Admitted Prior Art is silent as to whether this PLL frequency synthesizer is part of a transmitter-receiver even though such would be inherent.

However, Jokura teaches in Fig. 2, a PLL synthesizer as part of a transmitter-receiver (col. 3, lines 27-64).

One skilled in the art would have clearly recognized that a PLL synthesizer as part of a

transmitter-receiver is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Jokura to the invention as described in Applicant's Admitted Prior Art to incorporate power-saving features in a mobile unit (col. 1, lines 10-16; lines 60-64).

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in combination with Jokura (US Patent 5,541,929) applied to claim 9 above, and further in view of Yoshinaka (US Patent 5, 877,657).

As noted above Applicant's Admitted Prior Art in combination with Jokura disclose all limitations of claim 9.

They do not however disclose wherein frequency-dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other.

However, Yoshinaka teaches a PLL clock generator wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other (col. 5, lines 34-55).

One skilled in the art would have clearly recognized that a PLL clock generator wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Yoshinaka to the invention as described in Applicant's Admitted Prior Art to provide a low cost

clock generator, eliminate extra terminals and allow frequency dividing ratios to be freely performed (col. 2, lines 34-40).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Hayashi et al. U. S. Patent 6,493,305 B1 a pulse width control circuit.

b. Ho U. S. Patent 6,240,152 B1 discloses an apparatus and method for switching frequency modes in a phase locked loop system.

c. Westergren et al. U. S. Patent 5,423,076 discloses a superheterodyne transceiver with bilateral first mixer and dual phase locked loop frequency control.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

Lawrence B. Williams

lbw
April 14, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600